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Fehlerkorrektursystem

Système de correction d'erreurs

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- **PATENT ABSTRACTS OF JAPAN vol. 10, no. 79 (E-391)28 March 1986 & JP-A-60 223 334 (NEC) 7 November 1985**

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Description

BACKGROUND OF THE INVENTION

The present invention generally relates to a system for correcting an error through decoding of an error correction code and, more particularly, to an error correction decoder which performs its error correcting operation on a pipeline processing basis for each code block and which is suitably used in a digital magnetic recording/playback apparatus.

In the case of such a recording medium as magnetic tape on which a digital signal is recorded, when it is desired to play back the recorded data, e.g., "1" and "0", scars or dust on the tape sometimes cause erroneous playback of them as "0" and "1". As its countermeasure, there has been known a system in which a data is divided into a plurality of blocks each having a predetermined length and parity data is added to each block to form a codeword for an error correction code so that the data is recorded in the form of such codewords. In this case, its playback system includes an error correction decoder which performs its error correcting operation over each of the codewords sequentially read to realize right playback of the data.

The aforementioned error correcting operation includes a plurality of processing steps of generating a syndrome, deriving an error evaluation polynomial and an error location polynomial and evaluating error locations and error values. In typical one of conventional error correction decoders, the decoder has a plurality of blocks which execute the plurality of processing steps respectively as an allocated portion thereof, so that the plurality of blocks perform their pipeline processing operations over a plurality of codewords continuously received. Each block, according to a common control signal, transfers its processing result to the next block and starts processing of the next codeword. Such an example is an error correcting system as disclosed in JP-A-60-223334.

Fig. 2 shows a block diagram of a prior art error correcting system disclosed in The Journal of The Institute of Television Engineers of Japan Vol. 43, No. 12 (1989), pp.1333-1339. In the error correcting system, among the aforementioned plurality of processing steps of the error correcting operation, the processing steps of deriving error evaluation/location polynomials and evaluating error locations and values are allocated to an error location/evaluation block 12. In more detail, the error correcting system comprises a syndrome generation block 11, the error location/evaluation block 12 and a correction block 13. The codeword processings of the respective blocks are started under control of a common reset signal indicative of the leading head of the codeword. How to transfer the codewords between the blocks in the error correcting system is illustrated in Fig. 3. The reset signal is generated by detecting a synchronizing pattern recorded in the leading head of the codewords on a recording medium.

SUMMARY OF THE INVENTION

In such a system of correcting an error in each codeword based on the detected synchronizing pattern as mentioned above, generation of an out-of-synchronism condition causes generation of an incomplete codeword shorter than its normal codeword. With a helical scan type digital video tape recorder (VTR), in particular, reading operation is undesirably effected across a plurality of tracks having a codeword string recorded therein in a special playback mode, e.g., in a high-speed playback mode. Such a track shift causes an out-of-synchronism condition, thus resulting in generation of an incomplete codeword shorter than the normal codeword. At this time, an pulse interval in the reset signal is correspondingly shortened. With the above error correcting system, when the reset interval is shortened in this way, the processings of the error location/evaluation block 12 and correction block 13 are also aborted with the same interval. The codeword then being processed at the error/location/evaluation block is subjected at the correction block 13 to a wrong correcting operation based on intermediate processing values. Further, the codeword issued from the correction block 13 is missing in data because the correction block 13 shifts its correcting operation toward the next codeword in the course of its output operation. Such conversion of the codeword data to a wrong data based on the wrong correction or data missing is referred to as "miss-correction". Such miss-correction becomes a serious problem, for example, in picture image data because the miss-correction results in deterioration of its picture quality.

It is therefore an object of the present invention to eliminate such miss-correction problem as in the prior art to improve a reproduction data in reliability. This object is accomplished by the system defined in claim 1.

In accordance with an embodiment of the present invention, the invention comprises a plurality of processing blocks connected in cascade for executing as allocated a plurality of stages of error correction processings at least including generating syndrome symbols on the basis of a read codeword, deriving an error location polynomial and an error evaluation polynomial from the generated syndrome, evaluating error locations and error values according to the error location/evaluation polynomials, and correcting an error in the delayed codeword with use of the evaluated error locations and error values for output, in which the plurality of processing blocks start their processings of their next ones of the continuous codewords under control of their mutually independent control signals with use of processing results of their upstream processing blocks. That is, although the error correcting operation is carried out in the plurality of processing blocks on pipeline processing basis, but unlike the conventional pipeline operation, the processings of the respective blocks are effected under

control of individual control signals.

More particularly, a monitor unit which monitors on the basis of a reset signal indicative of the leading head of each of codewords in a codeword string whether or not each codeword has a normal length. Of the plural stages of processing blocks, the processing block for deriving at least error location/evaluation polynomials or for evaluating error locations and values receives the control signal passed through an inhibit gate so as to start its selective processing operation over the codeword decided as normal in codeword length by the aforementioned monitor unit. The codeword data correction block receives such a control signal as inhibits its correcting operation of a codeword shorter than a predetermined codeword length. With such an arrangement, the codewords having the normal length can be prevented from being aborted in the course of the processings of the error location/evaluation block and correction block. Accordingly, the aforementioned erroneous correction, which would occurred in the prior art, can be eliminated and thus a miss-correction probability can be reduced. Furthermore, the codeword shorter than the normal one can be inhibited from being subjected to such a miss-correction for separate processing.

Other objects and features of the present invention will be clear from the following detailed explanation in conjunction with embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram of an error correcting system in accordance with an embodiment of the present invention;

Fig. 2 is a block diagram of a prior art error correcting system;

Fig. 3 is a timing chart for explaining how to transfer codewords in the prior art error correcting system;

Fig. 4 is a block diagram showing a detailed arrangement of an error correcting system in accordance with another embodiment of the present invention;

Fig. 5 is a timing chart for explaining how to transfer codewords in the embodiment of Fig. 4;

Fig. 6 is a block diagram of an example of a delay means 18 in the embodiment of Fig. 4;

Fig. 7 is a block diagram of another example of the delay means 18 in the embodiment of Fig. 4;

Fig. 8 is a block diagram of an example of an (N+β) delay generating circuit 26 in Fig. 7; and

Fig. 9 is a block diagram of another example of the (N+β) delay generating circuit 26 in Fig. 7.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be detailed with reference to the attached drawings.

Referring first to Fig. 1, there is shown a block diagram of an error correcting system in accordance with an embodiment of the present invention for explaining the basic operation of the system. An input signal as a codeword for an error correcting code having parity symbols for error correction attached to each data block is continuously applied to a syndrome generation block 11 where syndrome data are computed for each block codeword. An error location/evaluation block 12 generates error and error location polynomials, solves them and derives error locations and error values in a data string therefrom. Allocated to the logical processing of the error location/evaluation block 12 is a processing time which corresponds to a one-codeword length. A correction block 13, which performs correcting operation with use of the derived error locations and error values, performs a correction to the signal train having the input codeword of the syndrome generation block 11 delayed by a time corresponding to a two-codeword length and outputs the data. These three blocks 11, 12 and 13 are controlled by outputs of control signal generation circuits 14 to 16 respectively. That is, the control signal generators 14 to 16 are used to control flows of data between the blocks 11, 12 and 13. A codeword length comparator 17 compares the interval of a reset signal indicative of the head of the codeword with a designated codeword length to judge whether or not the codeword length is normal. The aforementioned control signal generators 14 to 16 receive respectively the reset signal and an output of the codeword length comparator 17, and generate respectively a control signal for associated one of the blocks 11 to 13. With such an arrangement, even when a generation of a incompletely short codeword causes generation of a shorter interval of the reset signal, this will not have any influences on the codeword being processed in the error location/evaluation block 12 and the correction block 13.

Explanation will next be made as to a specific circuit configuration of the embodiment and its operation. Fig. 4 shows a block diagram of the present embodiment, in which the processing contents of the syndrome generation block 11, error location/evaluation block 12 and correction block 13 are the same as those in Fig. 1. A not illustrated reset signal generator detects a synchronizing pattern from the playback signal string to generate a synchronizing signal. The reset signal generator, when failing to detect the synchronizing pattern at the time that a time corresponding to the designated one synchronizing block length elapses after the previous synchronism detection (pull-out), also generates the synchronizing signal and searches a synchronizing pattern from the subsequent signal string. One synchronizing block consists of two codewords. Accordingly, the reset signal generator produce reset signals respectively indicating the leading heads of the two codewords on the basis of the synchronizng signal. When an pull-out synchronism condition takes place during playback op-

eration, there is generated an incomplete codeword which is shorter than the designated codeword length. The syndrome generation block 11, when receiving the reset signal from the not shown reset signal generator, terminates its syndrome generating operation, stores its result to a buffer and subsequently starts its syndrome generating operation over a newly entered codeword. A control signal C1 for instructing the error location/evaluation block 12 to start its logical operation is obtained by delaying the reset signal by a clock amount corresponding to codeword length N through a delay means 10 and then by passing it through a switch 20. A codeword length comparator 17 monitors the interval of the reset signal and when determining that the reset signal interval is shorter than a codeword length N, issues its output. During the output of the codeword length comparator 17, the switch is at its open position, whereby generation of the control signal C1 is inhibited. During the non-output of the comparator 17, the switch 20 is at its closed position, whereby the delayed reset signal is passed through the switch 20 as the control signal C1. Therefore, the error location/evaluation block 12 performs its error location/evaluating operation over the codeword of the designated codeword length N and does not perform its operation over incomplete codewords shorter than the designated codeword length N. On the other hand, a control signal C2 for instructing the correction block 13 to start its processing operation is obtained by delaying the reset signal by a clock amount corresponding to 2N through a delay means 18. Further, an input signal is also delayed by a clock amount corresponding to 2N through a delay memory 19 and then applied to the correction block 13. In addition, the correction block 13 receives the error locations and error values calculated at the error location/evaluation block 12 according to the control signal C2. In this way, the correction block 13 sequentially receives, corrects and outputs input signals. During the output period of a control signal C3, however, the correction block 13 does not perform its correcting operation and outputs sequentially received input signals as they are. The control signal C3 is generated by a delay means 21 which shifts an output of the codeword length comparator 17. The delay means 11 is made up of two stages of shift registers which use the control signal C2 as a shift clock. Accordingly, the correction block 13, so long as it receives an incomplete codeword shorter than the designated codeword length N, does not perform its correcting operation and outputs the original input signal as it is.

Shown in Fig. 5 is how the respective blocks perform their processing operation and their propagation states. In Fig. 5, one of sequentially entered codewords designated by 3' is an incomplete codeword shorter than the codeword length N. The syndrome generation block 11 sequentially generates syndromes for codewords 0, 1 and 2. Even at a time point t1 when the syndrome generation block 11 terminates its generation of a syndrome for the incomplete codeword 3', the error location/error evaluation block 12 does not receive the control signal C1 yet, which results in that the error location/error evaluation block 12 does not interrupt its logical error location/error evaluating operation over the codeword 2. This logical operation is terminated at a time point t2 and for a time period from t2 to t4, the error correction block 13 performs its correcting operation over the codeword 2. Therefore, it can be prevented that miss-correction is carried out based on an erroneous error location/error in the course of the logical operation. Since the switch 20 inhibits the output of the control signal C1 at the time point t2, the error location/error evaluation block 12 does not start its logical error location/error evaluating operation over the incomplete codeword 3' and starts its logical operation over a codeword 4 at a time point t3. Further, even when the reset signal is issued at the time point t1, the correction block 13 continues its correcting and outputting operation over the codeword 1, which results in that no data missing takes place. In a time period from t4 to t5, during which the incomplete codeword 3' shorter than the designated codeword length N is output, the control signal C3 inhibits the correcting operation, whereby the codeword 3' is output as it is. The data not subjected to the correction may be interpolated based on the data of the other normal codewords if necessary. In this way, in accordance with the present embodiment, since erroneous correction, which would has been caused by the processing start control of the respective blocks in the prior art, can be fully prevented, a miss-correction rate or probability can be reduced.

In the present embodiment, a time corresponding to the codeword length N is allocated to the logical processing of the error location/evaluation block 12 and the correction block 12 correspondingly corrects the signal delayed by a clock amount corresponding to 2N. If the number of clocks necessary for the logical processing of the error location/evaluation block 12 is denoted by γ ($\gamma < N$), then a delay for the delay means 18 and the delay memory 19 is expressed by $N + \beta$ ($\gamma \leqq \beta \leqq N$).

On the contrary, when the logical processing time up to the error location/evaluation is longer than the codeword length N, it becomes necessary to divide the error location/evaluation block 12 further into a plurality of sub-blocks to sequentially proceed a plurality of logical processing stages on a pipeline processing basis.

When input codewords have a fixed period N' which is longer than the codeword length, the reset signal appears at a period N' in a non-out-of-synchronism condition. In this case, the codeword length comparator 17 compares the designated codeword period N' with the period of the reset signal for monitoring. Suppose now that a delay for the delay means 10 is denoted by N' and delays for the delay means 18 and the delay memory 19 are denoted respectively by 2N'. Or suppose that if a relationship $\gamma < N'$ is satisfied, then a delay for the delay means 18 and the delay memory 19 is denoted by $N' + \beta$ ($\gamma \leqq \beta \leqq N'$).

Fig. 6 is an example of the structure of the delay

means 18, in which delay elements 22 corresponding in number to twice the maximum designatable codeword length are connected in cascade so that outputs of the respective delay elements 22 are connected to the inputs of a multiplexer 13. For selecting a delay corresponding to (N+β), the multiplexer 13 selects the outputs of the delay elements 22 according to a delay selection signal and generates an output as the control signal c2. The control signal c2 is used also as a reading start signal of the delay memory 19 in Fig. 4.

Referring to Fig. 7, there is shown another example of the structure of the delay means 18. In the present embodiment, a random access memory (RAM) 24 is used to delay the reset signal by an amount of (N+β). In other words, the RAM 24 performs its reading and writing operations at an identical address during one period of the input clock. An address generation binary counter 25 counts an input clock. An (N+β) frequency divider 26 generates a pulse having a period corresponding to (N+β) times the clock period and returns the address value of the address generation binary counter 25 to its initial value. That is, the address generation binary counter 25 outputs the same address value to the RAM 24 at a period of (N+β). A data read out from the RAM 24 at a give time point is a data written in the RAM 24 (N+β) clocks before. Accordingly, the RAM 24 delays the reset signal by (N+β) clocks to generate the control signal c2. Like the RAM 24, a second RAM for performing its reading and writing operations at an address designated by the binary counter 25 may be provided as the delay memory 19 for codewords.

Shown in Fig. 8 is an example of the structure of the (N+β) frequency divider 26 in Fig. 7. In the drawing, an adder 28 adds the designated codeword length N and a designated delay β together to generate a code indicative of a value (N+β-1). A binary counter 27 counts an input clock. A coincidence detecting circuit 29 returns the value of the binary counter 27 to its initial value 0 when the value of the binary counter 27 coincides with (N+β-1). Accordingly, an output of the coincidence detector 29 is a pulse signal having a period of (N+β). Such an arrangement may be employed that the binary counter 27 comprises a down counter, the coincidence detector 29 is replaced by a circuit for detecting that the output of the counter becomes "0", and an output of the circuit causes the output (N+β-1) of the adder 28 to be set at the down counter.

Fig. 9 is another example of the structure of the (N+β) frequency divider 26 in Fig. 7. In the example, the delay β is fixed at the codeword length N, that is, the frequency divider 26 is practically a 2N frequency divider. Further, the designated codeword length N is provided not directly but in the form of α^{N-1}, where α denotes an element on a Galois field. The power number (i) in α^i, i.e. the output of the Galois field down counter 30, is decreased by 1 for each clock usually through the multiplication operation on Galois field in a Galois field down counter 30. An α^0 detection circuit 31 outputs a pulse when the power number of the element as an output of the Galois field down counter 30 becomes zero. A binary counter 32 inverts its output each time the unit element detector 31 outputs the pulse. An AND gate 33 performs a logical "AND" operation of the output of the α^0 detection circuit 31 and the output of the binary counter 32. In other words, the AND gate 33 outputs the output of the α^0 detection circuit 31 once for its twice output. Accordingly, a output pulse signal is issued from the AND gate 33 at intervals of 2N. There may be possible to employ such an arrangement that the α^0 detection circuit 31 is replaced by a circuit for detecting α^{N-1} so that the output of this detection circuit causes the initial value of the Galois field counter to be returned to α^0.

As has been disclosed in the foregoing, in accordance with the present invention, since the miss-correction, which would has occurred in the prior art control, can be eliminated, a miss-correction probability can be reduced. This feature becomes highly effective, in particular, in a high-speed playback mode in which a dummy short codeword is often generated.

Claims

1. A system for correcting errors in sequentially read out codewords, comprising

   a plurality of processing blocks (11, 12, 13) connected in cascade and including

   a first processing block (11) for receiving each codeword and generating syndrome data on the basis of parity symbols contained in the codeword,
   a second processing block (12) for deriving an error location polynomial and an error evaluation polynomial for the syndrome data and solving the error location and evaluation polynomials to produce error location and error value data, and
   a third processing block (13) for correcting errors in the respective delayed codeword using said error location and value data, and outputting the corrected codeword, and

   means for generating control signals (c1, c2) to start the processing of the first to third processing blocks (11 ...13) on the basis of a synchronising signal indicating the head of each codeword,
   characterised by
   means (10, 18) for delaying the control signals (cl, c2) for the second and third processing blocks (12, 13) with respect to that for the first processing block (11), and
   means (17, 20) for inhibiting those control sig-

nals (c1) for the second processing block (12) which are based on the heads of codewords of incorrect lengths.

2. The system of claim 1, further comprising

a comparator (17) for outputting a signal whenever the length of the respective codeword being corrected has a predetermined value, and

delay means (21) for delaying the comparator output signal to generate an inhibit signal (c3) for inhibiting the error correction processing by the third processing block (13) for the period during which a codeword of incorrect length is applied to the third processing block (13).

3. The system of claim 1 or 2, wherein said means (18) for delaying the control signal (c2) for the third processing block (13) comprises a plurality of delay elements (22) connected in cascade and having their outputs connected to a multiplexer (23), the multiplexer (23) generating the control signal (c2) for the third processing block (13) on the basis of the output of one of said delay elements (22) selected in accordance with a delay selection signal.

4. The system of any preceding claim, wherein said means (18) for delaying the control signal (c2) for the third processing block (13) includes

a random access memory (24) for storing the control signal for said first processing block (11),
address generating means (25) for sequentially stepping up the address value for reading/writing from/to said random access memory (24), and
delay designating means (26) for returning the address value of said address generating means (25) to its initial value at regular intervals.

5. The system of claim 4, wherein said delay designating means (26) includes

power changing means (30) for receiving a signal indicative of the element (α^{N-1}) in a Galois field (where N equals the codeword length), changing the power number of the Galois field element in sequence and outputting the derived Galois field element,
power detecting means (31) for producing an output signal when the output of the power changing means (30) assumes a predetermined value, and
counter means (32) for counting the frequency of detections of the designated value by said power detecting means (31) and passing the output signal of said power detecting means (31) once for a constant detection frequency, so as to return said address value to its initial value dependent on the output of said counter means (32).

Patentansprüche

1. System zur Korrektur von Fehlern in sequentiell ausgelesenen Codewörtern, umfassend

mehrere in Kaskade geschaltete Verarbeitungsblöcke (11, 12, 13) mit

einem ersten Verarbeitungsblock (11) zur Aufnahme jedes Codewortes und zum Erzeugen von Syndromdaten aufgrund von in dem Codewort enthaltenen Paritätssymbolen,
einem zweiten Verarbeitungsblock (12) zum Ableiten eines Fehlerortungs- und eines Fehlerbewertungs-Polynoms für die Syndromdaten und zum Erzeugen von Fehlerort- und Fehlerwert-Daten durch Lösen der Fehlerortungs- und Fehlerbewertungs-Polynome, und
einem dritten Verarbeitungsblock (13) zur Korrektur von Fehlern in dem jeweiligen verzögerten Codewort unter Verwendung der Fehlerort- und Fehlerwert-Daten und zur Ausgabe des berichtigten Codeworts, und

eine Einrichtung zur Erzeugung von Steuersignalen (cl, c2) für den Beginn der Verarbeitung in den ersten bis dritten Verarbeitungsblöcken (11 ... 13) aufgrund eines den Kopf jedes Codewortes angebenden Synchronisiersignals, **gekennzeichnet** durch
eine Einrichtung (10, 18) zur Verzögerung der Steuersignale (cl, c2) für den zweiten und den dritten Verarbeitungsblock (12, 13) bezüglich derjenigen für den ersten Verarbeitungsblock (11) und
eine Einrichtung (17, 20) zum Sperren derjenigen Steuersignale (c1) für den zweiten Verarbeitungsblock (12), die auf Köpfen von Codewörtern unrichtiger Länge beruhen.

2. System nach Anspruch 1, ferner umfassend

einen Komparator (17) zum Ausgeben eines Signals, sooft die Länge des jeweils korrigierten Codewortes einen vorgegebenen Wert aufweist, und
eine Verzögerungseinrichtung (21) zur Verzögerung des Komparator-Ausgangssignals unter Erzeugung eines Sperrsignals (c3) zum

Sperren der Fehlerkorrekturverarbeitung durch den dritten Verarbeitungsblock (13) für die Zeitspanne, während der an dem dritten Verarbeitungsblock (13) ein Codewort unrichtiger Länge anliegt.

3. System nach Anspruch 1 oder 2, wobei die Einrichtung (18) zum Verzögern des Steuersignals (c2) für den dritten Verarbeitungsblock (13) mehrere in Kaskade geschaltete Verzögerungsglieder (22) aufweist, deren Ausgänge an einen Multiplexer (23) angeschlossen sind, wobei der Multiplexer (23) das Steuersignal (c2) für den dritten Verarbeitungsblock (13) aufgrund des Ausgangssignals eines entsprechend einem Verzögerungs-Wahlsignal ausgewählten Verzögerungsgliedes (22) erzeugt.

4. System nach einem der vorhergehenden Ansprüche, wobei die Einrichtung (18) zum Verzögern des Steuersignals (c2) für den dritten Verarbeitungsblock (13) aufweist:

einem Random-access-Speicher (24) zur Speicherung des Steuersignals für den ersten Verarbeitungsblock (11),
eine Adressen-Erzeugungseinrichtung (25) zum sequentiellen Weiterschalten des Adreßwertes zum Lesen/Schreiben in den/aus dem Random-access-Speicher (24), und
eine Verzögerungs-Bestimmungseinrichtung (26), die den Adreßwert der Adressen-Erzeugungseinrichtung (25) in regelmäßigen Intervallen auf seinen Ursprungswert zurückführt.

5. System nach Anspruch 4, wobei die Verzögerungs-Bestimmungseinrichtung (26) aufweist:

eine Potenzänderungseinrichtung (30) zur Aufnahme eines Signals, das das Element (α^{N-1}) in einem Galois-Feld angibt (wobei N gleich der Codewortlänge ist), zum sequentiellen Ändern der Potenzzahl des Elements in dem Galois-Feld, und zur Ausgabe des so abgeleiteten Elements des Galois-Feldes,
eine Potenz-Erfassungseinrichtung (31) zur Erzeugung eines Ausgangssignals, wenn der Ausgang der Potenz-Änderungseinrichtung (30) einen vorgegebenen Wert annimmt, und
eine Zähleinrichtung (32), die die Häufigkeit ermittelt, mit der die Potenz-Erfassungseinrichtung (31) den vorgegebenen Wert erfaßt, und das Ausgangssignal der Potenz-Erfassungseinrichtung (31) bei konstanter Erfassungsfrequenz einmal weitergibt, um den Adreßwert in Abhängigkeit vom Ausgangssignal der Zähleinrichtung (32) auf seinen Ursprungswert zurückzuführen.

Revendications

1. Système pour corriger des erreurs dans des mots de code lus séquentiellement, comprenant

une pluralité de blocs de traitement (11,12,13) branchés en cascade et comprenant
un premier bloc de traitement (11) pour recevoir chaque mot de code et produire des données de syndromes sur la base de symboles de parité contenus dans le mot de code,
un second bloc de traitement (12) pour dériver un polynôme de repérage d'erreurs et un polynôme d'évaluation d'erreurs pour les données de syndromes et résoudre les polynômes de repérage et d'évaluation d'erreurs pour produire des données d'emplacements d'erreurs et de valeurs d'erreurs,
un troisième bloc de traitement (13) pour corriger des erreurs dans le mot de code respectif retardé en utilisant lesdites données d'emplacements et de valeurs d'erreurs, et délivrer le mot de code correct, et
des moyens pour produire des signaux de commande (c1,c2) pour faire démarrer le traitement des premier, second et troisième blocs de traitement (11...13) sur la base d'un signal de synchronisation indiquant l'entête de chaque mot de code,
caractérisé par
des moyens (10,18) pour retarder les signaux de commande (c1,c2) pour les second et troisième blocs de traitement (12,13) par rapport aux signaux de commande pour le premier bloc de traitement (11), et
des moyens (17,20) pour bloquer les signaux de commande (c1) pour le second bloc de traitement (12), qui sont basés sur les en-têtes de mots de code possédant des longueurs incorrectes.

2. Système selon la revendication 1, comprenant en outre

un comparateur (17) pour délivrer un signal chaque fois que la longueur du mot de code respectif, qui est corrigé, possède une valeur prédéterminée, et
des moyens de retardement (21) pour retarder le signal de sortie du comparateur pour produire un signal de blocage (c3) pour bloquer le traitement de correction d'erreurs exécuté par le troisième bloc de traitement (13) pendant l'intervalle de temps, pendant lequel un mot de code ayant une longueur incorrecte est appliqué au troisième bloc de traitement (13).

3. Système selon la revendication 1 ou 2, dans lequel

lesdits moyens (18) pour retarder le signal de commande (c2) pour le troisième bloc de traitement (13) comprennent une pluralité d'éléments de retardement (22) branchés en cascade et dont les sorties sont connectées à un multiplexeur (23), le multiplexeur (23) produisant le signal de commande (c2) pour le troisième bloc de traitement (13) sur la base du signal de sortie de l'un desdits éléments de retardement (22) sélectionné en fonction d'un signal de sélection de retard.

4. Système selon l'une quelconque des revendications précédentes, dans lequel lesdits moyens (18) pour retarder le signal de commande (c2) pour le troisième bloc de traitement (13) comprennent

une mémoire à accès direct (24) pour mémoriser un signal de commande pour ledit premier bloc de traitement (11),
des moyens (25) de production d'adresses pour augmenter pas-à-pas séquentiellement la valeur de l'adresse pour la lecture/l'écriture dans ladite mémoire à accès direct (24), et
des moyens de désignation de retard (26) pour ramener la valeur d'adresse desdits moyens (25) de production d'adresses, à sa valeur initiale, à des intervalles réguliers.

5. Système selon la revendication 4, dans lequel lesdits moyens (26) de désignation de retard comprennent

des moyens (30) de modification de puissance pour recevoir un signal indicatif de l'élément (N-1) dans un espace de Galois (N étant égal à la longueur du mot de code), modifier séquentiellement la valeur de la puissance de l'élément de l'espace de Galois et délivrer l'élément dérivé de l'espace de Galois,
des moyens (31) de détection de puissance pour produire un signal de sortie lorsque le signal de sortie desdits moyens de modification de puissance (30) comprend une valeur prédéterminée, et
des moyens de comptage (32) pour compter la fréquence de détections de la valeur désignée par lesdits moyens (31) de détection de puissance et transmettre le signal de sortie desdits moyens (31) de détection de puissance une fois pour une fréquence de détection constante de manière à ramener ladite valeur d'adresse à sa valeur initiale en fonction du signal de sortie desdits moyens de comptage (32).

FIG.1

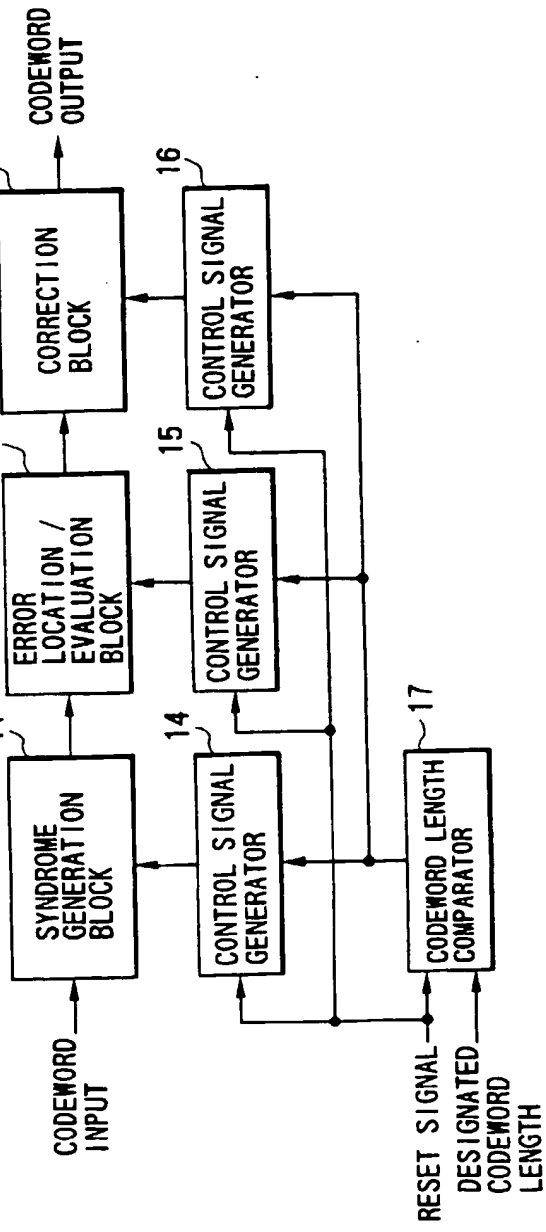

FIG.2 PRIOR ART

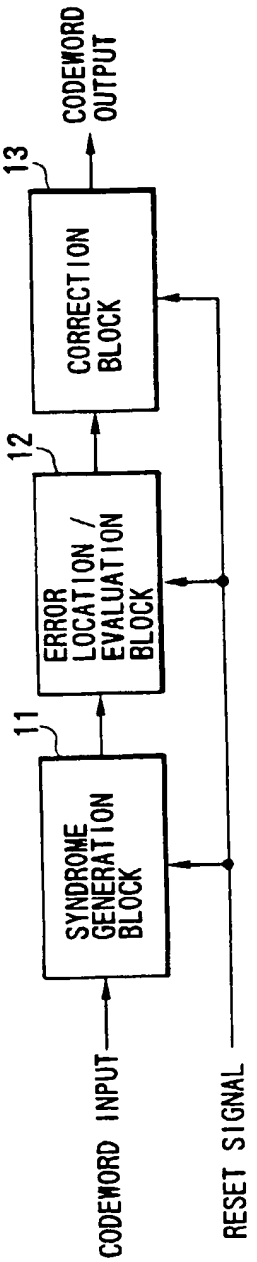

FIG.3 PRIOR ART

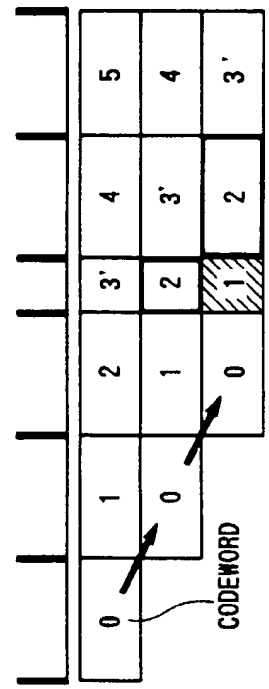

FIG.4

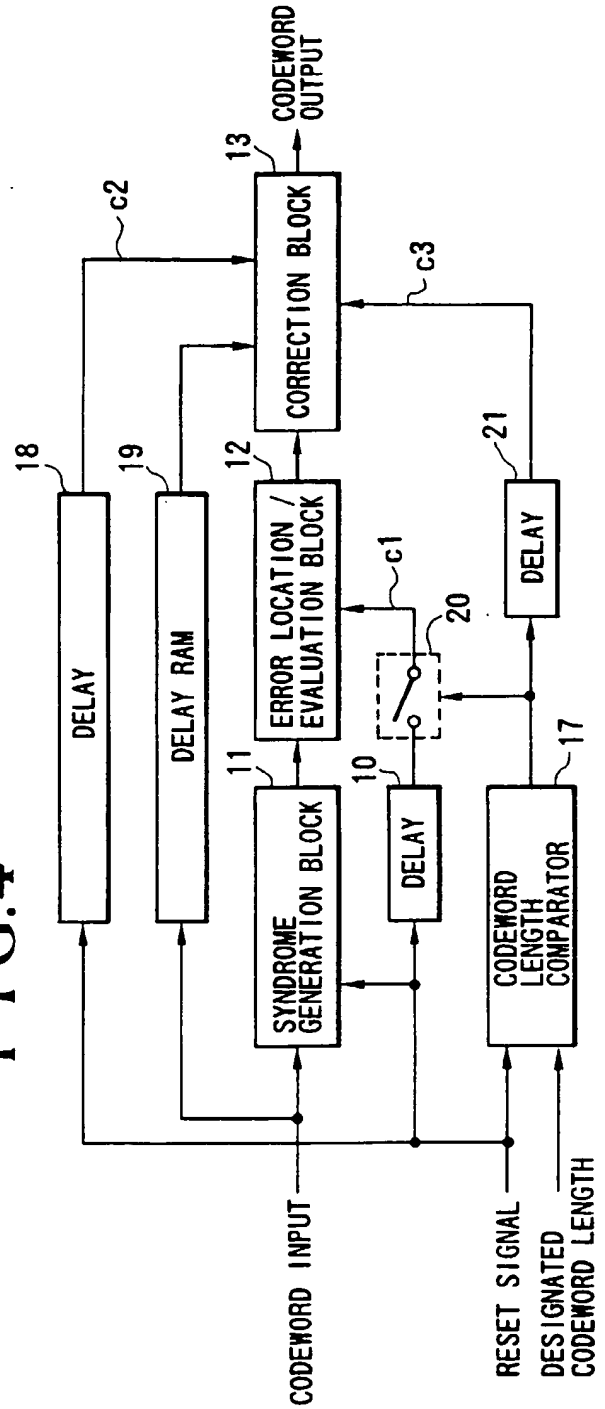

FIG.5

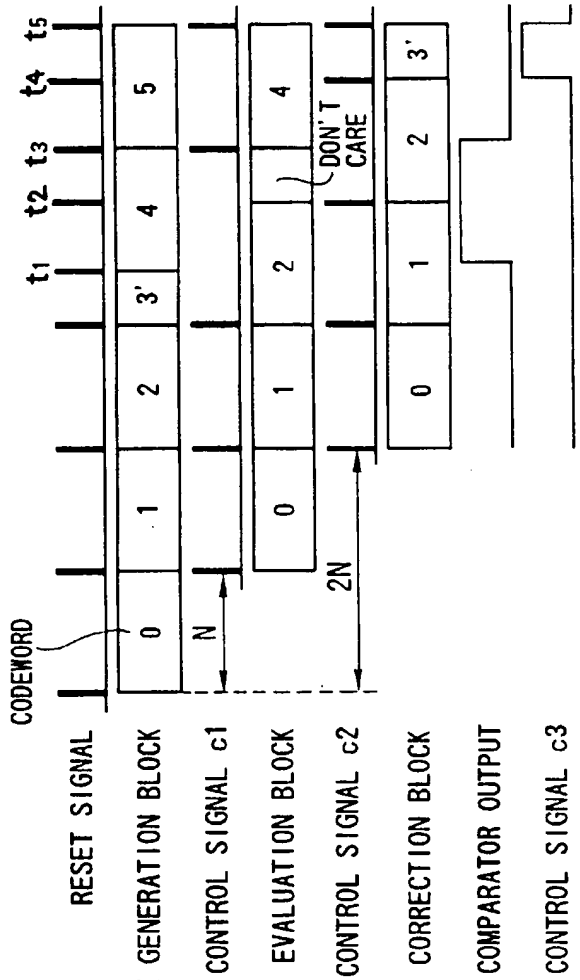
RESET SIGNAL
SYNDROME GENERATION BLOCK
CONTROL SIGNAL c1
ERROR LOCATION / EVALUATION BLOCK
CONTROL SIGNAL c2
CORRECTION BLOCK
CODEWORD LENGTH COMPARATOR OUTPUT
CONTROL SIGNAL c3
CODEWORD
N
2N
DON'T CARE
t1
t2
t3
t4
t5
0
1
2
3'
4
5

FIG.6

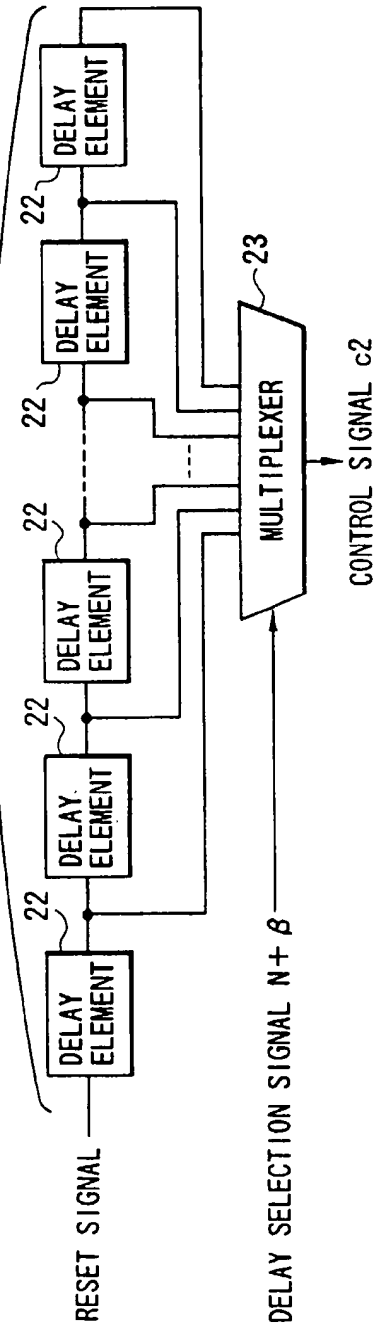
2N'
RESET SIGNAL
DELAY ELEMENT
22
MULTIPLEXER
23
DELAY SELECTION SIGNAL N+β
CONTROL SIGNAL c2

FIG.7

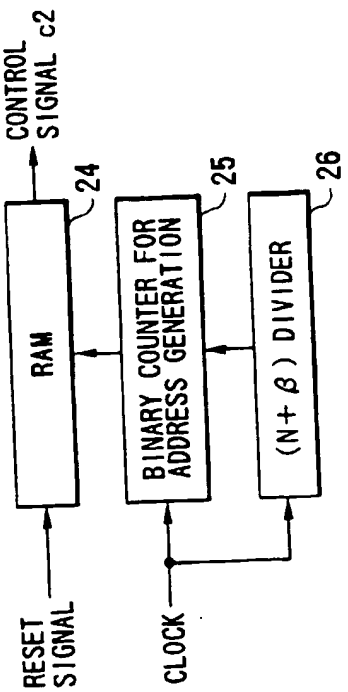

FIG.8

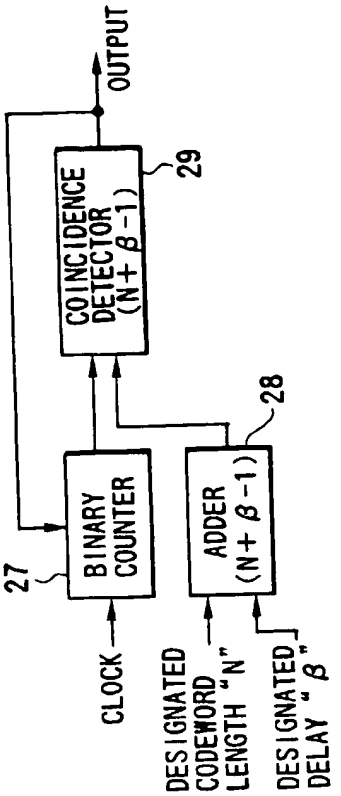

FIG.9